



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,856	10/08/2003	Chiaming Chai	BUR9-1999-0287-US2	7132
30449	7590	06/14/2005	EXAMINER	
SCHMEISER, OLSEN + WATTS 3 LEAR JET LANE SUITE 201 LATHAM, NY 12110			CHAUDRY, MUJTABA M	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/681,856

Applicant(s)

CHAI ET AL.

Examiner

Mujtaba K. Chaudry

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 4, 7, 12-15, 17, 18 and 20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4, 7, 12-15, 17, 18 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 October 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Double Patenting

The Double-Patenting rejection in prior office action is hereby withdrawn due to approval of terminal disclaimer filed June 8, 2005.

Response to Amendment

Applicants amendments with respect to amended claims 1, 7 and 12, previously presented claims 4, 13-15, 17, 18 and 20 filed March 30, 2005 have been fully considered but are not persuasive. Claims 2-3, 5-6, 8-11, 16 and 19 have been cancelled and withdrawn from consideration. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicants contend, "...the present application is a divisional of issued USPN 6658610...independent claims 1, 7 and 12 have been amended to include all of the limitations of corresponding independent claims 1, 5 and 8 of USPN 6658610..." The Examiner agrees. A terminal disclaimer has been received and accepted which overcomes the double patenting rejection only. However, the Examiner would like to point out that the prior art rejection with respect to the Adams patent, USPN 5535164 is not overcome and there is no attempt to point out novelty in the response filed March 30, 2005. See MPEP 714.04. It is the Examiner's conclusion that the pending claims in the present application, as presented, are not patentably distinct over the prior art of record, namely Adams, USPN 5535164.

Art Unit: 2133

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claims 1, 7 and 12 and previously presented claims 4, 13-15, 17, 18 and 20. Full consideration has given. It is the Examiner's conclusion that amended claims 1, 7 and 12 and previously presented claims 4, 13-15, 17, 18 and 20 are not patentably distinct or non-obvious over the prior art of record. See office action, below.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 4, 7, 12-15, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al. (USPN 5535164) further in view of AAPA.

As per claims 1, 7, 12 and 17, Adams et al. (herein after: Adams) substantially teaches (title and abstract) a single BIST which can test various memories of different sizes, types and characteristics by using a state machine to select and generate all patterns required for testing all of the memories on the chip, and impressing all of the data, including expected data, and address information on all of the memories simultaneously. The BIST also generates unique (separate) control signals for the various memories and impresses these control signals on the various memories. The BIST selectively asserts the various control signals so as to apply (write) the data

Art Unit: 2133

and to read and capture (load result) failure information only to/from those memories whose unique controls are asserted. Selective assertion of a memory's write enable signal prevents multiple writes to a location which can potentially mask cell write and leakage defects while selective assertion of a memory's load result signal is performed only when valid memory output data is expected so as not to capture false error information. The control signals instruct those memories that do not use a particular sequence of inputs or any portion of a given sequence of inputs to "ignore" such signals, thereby generating the necessary signals to form the test patterns for each and every memory, the data and address information for those patterns, the control signals to write and read each memory, and capture error information for that particular memory. A single BIST can be used to test a multiplicity of memories of different sizes and different types. Selective assertion of a memory's write enable signal prevents multiple writes to a location which can potentially mask cell write defects and cell leakage defects. Selective assertion of a memory's load result signal prevents capture of a false fail signal due to potentially inverted data stored in the memory in the second and subsequent address accesses. Adams teaches (col. 3, lines 20-56) the BIST circuit 10 shuts off each memory's WE and LR signals as the current address exceeds that memory's address space and whenever else appropriate according to the individual memory's function. Shutting off the WE prevents rewriting memory locations through a particular pattern. Rewriting a memory can potentially mask charge leakage problems in the cells. When the maximum address is reached, the state machine enters a WAIT state, resets the address counter, and performs various updates, including the assertion of a new subcycle. Furthermore, Adams teaches (col. 4, line 57—col. 5, lines 1-16) a content addressable memory (CAM) 24. The memory 24 is a 512 X 10 bit memory, with the 512 entries broken up into

groups of eight 10-bit comparators. A content addressable memory (CAM) is one in which binary data written therein is stored at the various address locations, but in this embodiment said stored data cannot be directly read out. The Cam memory performs the function of comparing binary data asserted thereon to determine if it has a particular bit pattern stored therein. If a pattern is so stored, the CAM memory responds by outputting an appropriate output signal, e.g., a binary "1", and if the pattern is not stored, a binary "0", on the output of each comparator depending on the data stored. Expressed another way, the CAM memory 24 acts as a comparator in which bits are stored in pre-selected patterns which correspond to portions of an address for another memory, and when a bit pattern is impressed on the CAM 24, the CAM 24 compares the impressed bit pattern with the stored bit patterns to determine if the particular bit pattern is stored, and which one of eight comparators found the bit pattern. Thus, the test function of the CAM requires an inputting of various test data and then performing a compare function between data stored therein and binary test data impressed thereon and determining if the output response is appropriate to indicate such a stored data being present at a given location or not.

Adams does not explicitly teach the address comparator to be a "compilable address magnitude comparator" as stated in the present application.

However, the specification on the present application teaches (specification, pages 1-4), in part, the compilable magnitude comparator address comparator overrides the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory. The Examiner would like to point that Adams teaches, as previously stated, a single BIST which can test various memories of different sizes, types and characteristics, wherein the BIST shuts off each memory's WE and LR signals as the current address exceeds that memory's address space and

Art Unit: 2133

whenever else appropriate according to the individual memory's function. Shutting off the WE prevents rewriting memory locations through a particular pattern. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Adams by incorporating a "compilable address magnitude comparator" within the method and apparatus. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by making the address magnitude compilable would enable it to efficiently override the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory.

As per claims 13 and 14, Adams substantially teaches, in view of above rejections, (cols. 11-13) comparing the rows and columns against maximum thresholds. The Examiner would like to point out the functionality if the row and column comparator is inherently included since both rows and columns are compared.

As per claims 4 and 15, Adams substantially teaches, in view of above rejections, a single BIST which can test various memories of different sizes, types and characteristics, wherein the BIST shuts off each memory's WE and LR signals as the current address exceeds that memory's address space and whenever else appropriate according to the individual memory's function. Shutting off the WE prevents rewriting memory locations through a particular pattern.

As per claims 18 and 20, Adams substantially teaches, in view of above rejections, a single BIST which can test various memories of different sizes, types and characteristics by using a state machine to select and generate all patterns required for testing all of the memories on the chip, and impressing all of the data, including expected data, and address information on all of the memories. The BIST selectively asserts the various control signals so as to apply

Art Unit: 2133

(write) the data and to read and capture (load result) failure information only to/from those memories whose unique controls are asserted. Selective assertion of a memory's write enable signal prevents multiple writes to a location which can potentially mask cell write and leakage defects while selective assertion of a memory's load result signal is performed only when valid memory output data is expected so as not to capture false error information. The control signals instruct those memories that do not use a particular sequence of inputs or any portion of a given sequence of inputs to "ignore" such signals, thereby generating the necessary signals to form the test patterns for each and every memory, the data and address information for those patterns, the control signals to write and read each memory, and capture error information for that particular memory. A single BIST can be used to test a multiplicity of memories of different sizes and different types. Selective assertion of a memory's write enable signal prevents multiple writes to a location which can potentially mask cell write defects and cell leakage defects. Selective assertion of a memory's load result signal prevents capture of a false fail signal due to potentially inverted data stored in the memory in the second and subsequent address accesses.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.


Mujtaba Chaudry
Art Unit 2133
June 09, 2005


ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100